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AM Shende - 1991 - adsabs.harvard.edu

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E Christen, K Bakalar - IEEE Transactions on Circuits and Systems II: Analog and ..., 1999 - ieeexplore.ieee.org

... Analog **simulation**, hardware description lan- guages, mixed-signal **simulation**, VHDL-AMS. ... HDL's can be divided into **digital**, **analog**, and mixed- signal HDL's ...

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**A Module Generator for High-Speed CMOS Current Output Digital/Analog Converters** - group of 4 »

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... California, Berkeley Abstract This paper presents a module generator for **Digital/Analog** Converter (DAC) circuits. A combination of circuit **simulation** and ...

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JF Andrews - Biotechnology and Bioengineering, 1968 - doi.wiley.com

... However, these equations can be solved using the analog computer or one of the **digital-analog simulation** prgrams..' The solutions presented in this paper were ...

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... **Fault Simulation** of Linear Analog Circuits ... An efficient **simulation** is then performed on this discretized circuit for the given input test wave form. ...

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[Physical and scalable IV model in BSIM 3 v 3 for \*\*analog/digital\*\* circuit simulation - group of 4 »](#)

Y Cheng, MC Jeng, Z Liu, J Huang, M Chan, K Chen, ... - IEEE Transactions on Electron Devices, 1997 - [ieeexplore.ieee.org](#)  
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JJ Liou, CS Ho, CG Christodoulou, L Chan - Proceedings of SPIE, 1995 - adsabs.harvard.edu

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NK Verghese, TJ Schmerbeck, DJ Allstot - 1995 - books.google.com

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T Austin - PROC INT TEST CONF., IEEE, IEEE SERVICE CENTER, PISCATAWAY, ..., 1993 - ieexplore.ieee.org

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... illustrating them by examples. Index Terms— Analog simulation, hardware description lan- guages, mixed-signal simulation, VHDL-AMS. ...

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Electsical Engineering Department, Stanford University Stanford, CA 94305 5 ...

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... any of the proposed standards. And, we do not cover analog and mixed-signal simulation strategies. These are much more mature than ...

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... signal circuits has been plagued by a num- ber of issues, the most important being:

1. Mixed-signal system simulation at the transistor level is CPU intensive. ...

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CF Chen, CY Lo, HN Nham, P Subramaniam - Proceedings of the 21st conference on Design automation, 1984 - [portal.acm.org](#)

... and a switch level approach for unit delay simulation. It provides logic and timing verification for general MOS circuits in a mixed-mode environment. ...

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J Haugeland - Mind design, 1981 - bi.snu.ac.kr  
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